

The diagram illustrates a system architecture with the following components and connections:

- CPU (10):** The central processing unit.
- Control Logic (28):** Receives **UPPER ADDR** and **DS** (32) from the CPU. It outputs **R/W** (30), **OE** (36), **DIR** (38), **R/W** (40), **DS** (42), and **CS** (44) to the I/O Device.
- Buffer Bus Hold (24):** Receives **Address** (20) from the CPU and **\overline{CS}** from the CPU. It outputs **Address** (22) to the I/O Device.
- Trceiver Bus Hold (18):** Receives **Data** (12) from the CPU and **OE** (36) from the Control Logic. It outputs **Data** (14) to the I/O Device.
- I/O Device (16):** The peripheral device that receives **Address** (22), **Data** (14), and control signals (**R/W**, **DS**, **CS**) from the CPU and Control Logic.

FIGURE 1

00T22T 0T2T20

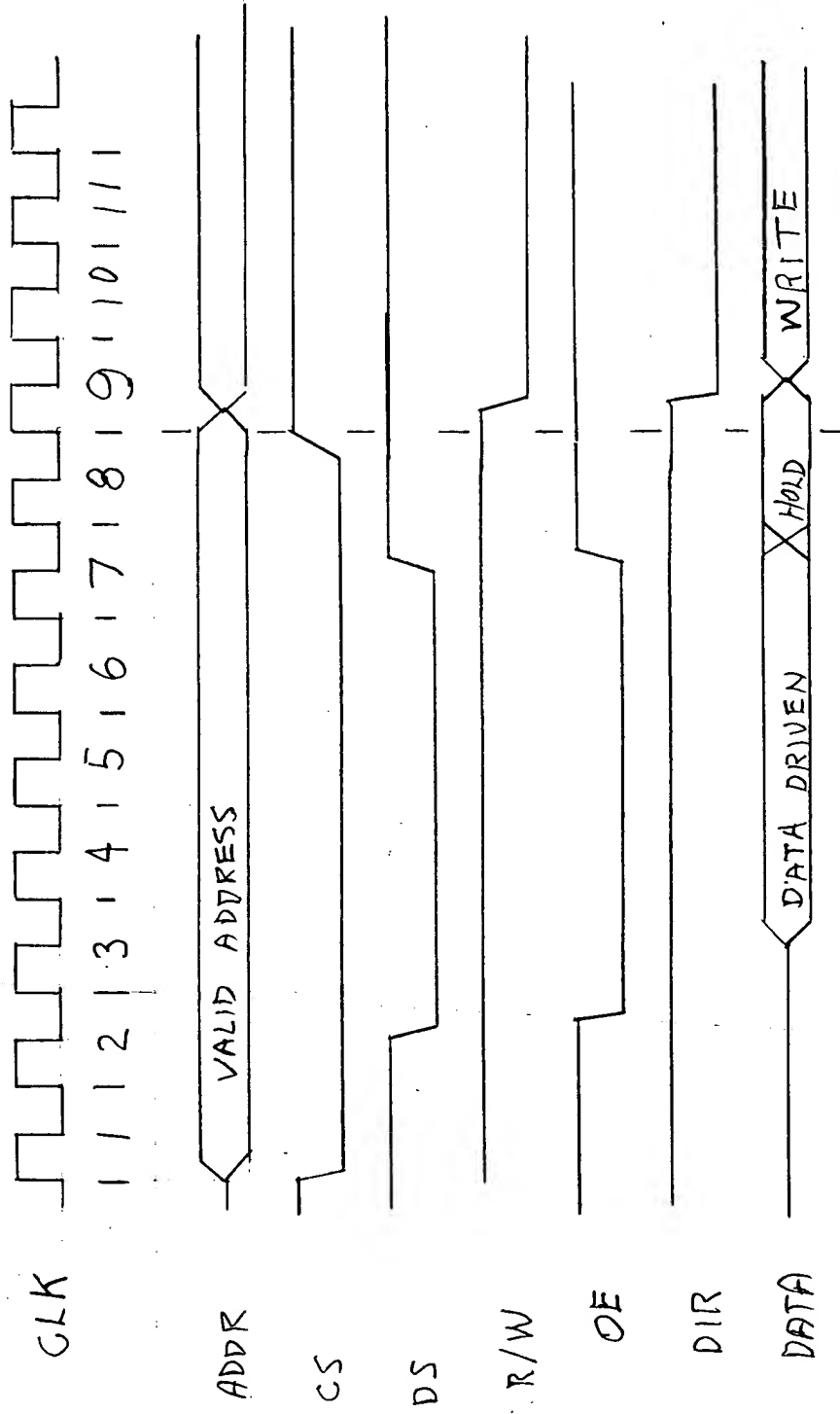


FIGURE 2